## Tentative EE 3300 Daily Coverage and Reading Materials - Fall 2024

Suggested Reading Materials are listed on a weeklly basis. Chapter references are to the Weste Harris test. See Table of Contents for specific sections.

Topics (exam dates not shown)

			Period	
Week	26-Aug	1	1 2 3	Chapter 1, Notes Electronic systems overview, economic opportunities Design approaches, yield and cost of semiconductor products Physical characteristics, soft faults
Week	2-Sep	2	4 5	Chapter 1, Notes Holiday Digital systems - basic gates, switch-level MOS models Digital systems - complex logic gates, pass transistor logic, Improved switch-Level MOS model
Week	9-Sep	3	6 7 8	Chapter 1, Notes Paramater extraction for Imp. switch-level model, propagation delay in logic, placement, stick diagrams Technology files, design rules, layout Fabrication technology, processing steps
Week	16-Sep	4	9 10 11	Chapter 1 Chapter 3, Chapter 6, Notes Fabrication technology, processing steps Interconnects - resistive and capacitive Back-end technology; packaging, bonding, basic semiconductorpProcesses
Week	23-Sep	5	12 13 14	Chapter 2 Chapter 6, Notes Devices/Device Models in semiconductor proceses - resistors, diodes Diode operation, diode model (diode equation), simplified diode models Exam 1
Week	30-Sep	6	15 16 17	Chapter 2, Chapter 3, Notes Diode applications, capacitor types and models, MOSFET operation MOSFET Operation - square law model, short channel model, BSIM model (brief) MOS process description - (n-channel, p-channel, capacitors, resistors)
Week	7-Oct	7	18 19 20	Notes Small feature MOS processes, bipolar devices, operation, device models Bipolar process description - (vertical and lateral devices, JFET, diffused resistor, varactor, diode) Bipolar devices - JFET and Thyristors
Week	14-Oct	8	21 22 23	Notes Bipolar devices - JFET and Thyristors Thyristors Amplification in transistor circuis
Week	21-Oct	9	24 25 26	Notes Amplification in transistor circuits Small-signal principles, ss equivalent circuits, ss diode model Exam 2
Week	28-Oct	10	27 28 29	Notes Small-signal models of n-terminal devices, MOSFET and BJT ss models Application of ss models, graphical analysis of nonlinear transistor circuits, comparison of MOS and BJT amplifiers Basic amplifier structures-CS/CE, CD/CC, CG/CB
Week	4-Nov	11	30 31 32	Notes High gain amplifiers - cascoding, cascading Current source biasing, darlington configuration Current sources and mirrors
Week	11-Nov	12	33 34 35	Chapter 9, Notes Differential amplifiers (brief), bipolar and MOS mappings Heirarchiacal digital design - behavioral, structural, physical, digital design flows Basic gates, charatristics of logic families
Week	18-Nov	13	36 37 38	Chapter 9, Notes Inverter pair, analysis of CMOS inverter Other CMOS logic circuits, static power dissipation, propatagion delay Exam 3
Week	2-Dec	14	39 40 41	Chapter 4, Notes The Reference Inverter, sizing of gates Propagation delay in multiple levels of logic, asymetric overdrive, optimally driving large capacitive loads Optimally driving large capacitive loads
Week	9-Dec	15	42 43 44	Chapter 4, Notes Logic effort, Elmore delay, power dissipation in logic circuits Sequential logic - latches, flip flops, shift registers, array logic, memory structures High frequency MOS model